A Comparison Between Sub-threshold and Adiabatic Power Saving Techniques

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ABSTRACT

This paper analyzes the difference between two techniques of power saving circuit design. As the number of transistors increases power consumption and the need for more power efficient products increases there is greater motivation to design circuits to fulfill these expectations. We will give a comparison between these two technologies using an adder as the basic circuit. We will compare the power output between different values of V_{DD} set at sub-threshold. We will compare several different styles of adiabatic techniques. We will compare the power consumption of an adiabatic adder run at sub-threshold and see how it will perform.

1. INTRODUCTION

Power consumption is rapidly becoming a limiting factor in integrated circuit technology as device sizes shrink. Applications such as wireless sensors, RFID tags, and similar devices have only a very small amount of power available to them, and must be designed to use a minimum of energy. Computer processors have massive amounts of power available, but can fail or become permanently damaged if the energy they dissipate causes severe heating. In an attempt to address these concerns, we have tested the effectiveness of two low-power techniques, sub-threshold biasing and adiabatic charging, in the design of a 16-bit carry lookahead adder.

1.1 Sub-threshold biasing

The concept of sub-threshold is fairly simple to understand, though the physics behind it can be daunting. In traditional CMOS processes the voltage threshold is the value for which the transistor is off. If the voltage potential from the transistors drain to source is below the threshold voltage this concept of the device being off is still considered true. However, in reality the transistor still retains it on off abilities at these low levels, because the current doesnt completely shut off, it is diminished exponentially [2]. Though the transistor will not perform at the level it was designed for it will still operate similarly. We will show how our circuit performed with different V_{DD} values set below the voltage threshold.

1.2 Adiabatic charging

Adiabatic switching occurs when no energy is dissipated as heat during switching events. Although leakage currents have become increasingly important with shrinking MOSFET sizes, the dominant power dissipation in modern electronic circuits remains the result of charging and discharging parasitic capacitances during switching. The standard CMOS inverter, for example, dissipates energy equal to:

$$E = \frac{1}{2}CV_{DD}^2$$

each time its output switches, where C is the total of the parasitic capacitances. As the inverter's inputs change, either the pull-up or pull-down network (PUN or PDN) will become conductive, and the internal capacitance will charge either to V_{DD} or 0 V. This process causes a large current to flow through the finite resistance R_{on} of the PUN or PDN, which causes heating and power dissipation. By replacing the voltage source V_{DD} with a constant current source, the rate at which charge is moved from the supply to the parasitic capacitance can be slowed down. Then, the energy dissipated during a pull-up event becomes:

$$E = PT = I^2RT = (\frac{CV_{DD}}{T})^2RT$$

$$E = \frac{R_{on}C}{T}CV_{DD}^2$$

where P is power and T is time [4]. Notice the energy dissipation asymptotically aproaches 0 as the switching time increases. This is consistent with the thermodynamic definition of an adiabatic process, in which the energy dissipation approaches 0 as the system is slowed down.

During pull-down events the same logic applies, and charge is slowly moved off the parasitic capacitance, back to the power supply. For this to be useful, the adiabatic power supply must be capable of absorbing the energy during pull-down events, as well as delivering energy during pull-up events. These supplies are often refered too as power clocks, since they serve to transfer power and control timing within the circuit.

2. EXPERIMENTAL RESULTS

In order to maintain fairness across the experiments, all simulations were conducted at a frequency of 20 MHz, and uti-

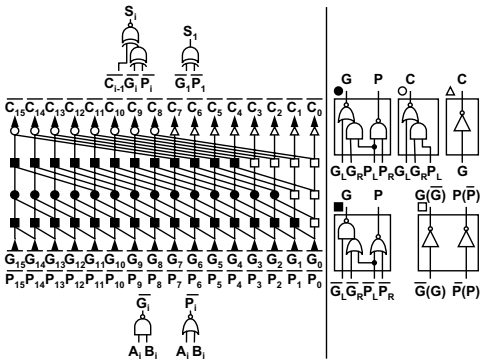

Figure 1: Carry Look-Ahead Adder

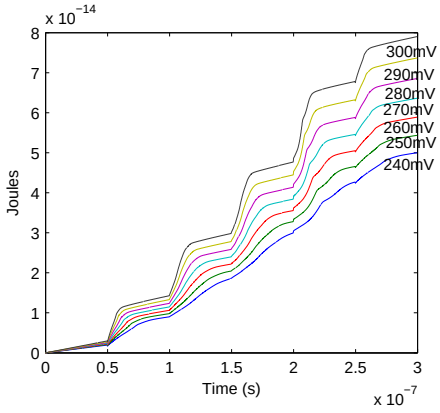

Figure 2: This shows the power consumption between V_{DD} ranges 240mV and 300mV for the sub-threshold adder.

lizing the same inputs to the adder: A0=0000h, A1=C690h, A2=6642h, A3=0C14h; B0=0000h, B1=944Eh, B2=4D3Eh, B3=7BE7h. All simulations were performed using the PTM 65 nm models.

2.1 Sub-threshold Biasing

In order to evaluate sub-threshold devices we implemented a simple adder based on a design by [1]. We chose this adder for simplicity as well as its effective way of alternating between regular and inverted values. Figure(1) shows the 16 bit implementation we used. The threshold voltage for the N-MOS device is 423mV and the P-MOS device is 365 mV. Throughout testing and simulations V_{DD}s max was 300mV to keep it well below threshold voltage.

We then swept the V_{DD} value from 300 mV down to 240 mV. We found that given our circuit and the frequency we were running at 240 mV was the lowest V_{DD} we could use. We ran a power consumption analysis on each of the test run for 300 ns. See Figure(2). It is easy to see from the figure that each successive 10mV jump increases the amount of energy drastically. Over a longer period of time that increase will become more and more apparent.

2.2 Adiabatic Charging

2.2.1 ECRL

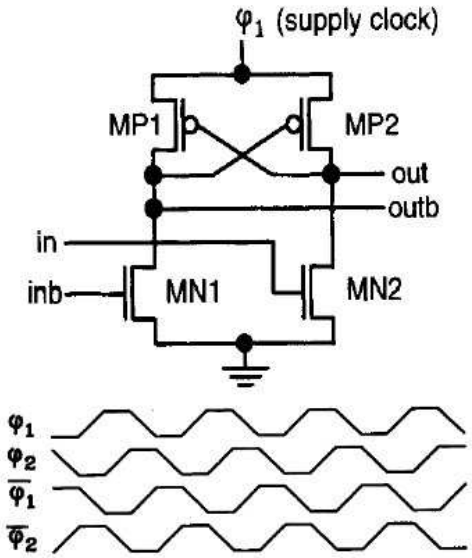

Figure 3: ECRL gate

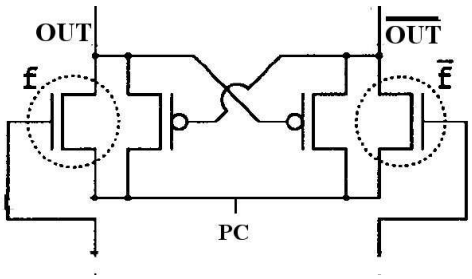

Figure 4: PAL gate

Efficient charge recovery logic (ECRL) is one possible implimentation of adiabatic logic [5]. The individual logic gates are essentially differential cascode voltage switch logic (DCVSL) gates, but with the supply connection replaced by a trapezoid shaped power clock. On the rising edge of the clock, the parasitic capacitance of the gate is slowly charged from 0 up to V_{DD}, at which point its outputs are valid, and then slowly charged back down from VDD to 0 V, recovering energy. Four clocks are required to create a pipeline of ECRL gates, in which each subsequent stage begins charging up from 0 V to VDD after the output of the previous stage has become stable. Once a stage has charged to VDD its outputs will remain stable, and the previous stage can be charged back down to 0 V. An ECRL gate and the appropriate clocks are shown in Figure (3).

One disadvange to the ECRL style is that PMOS transistors do not pass a strong 0 V, and as a result the outputs do not charge all the way down to 0 V when the power clock discharges. When the gate inputs activate switch, this unrecovered charge will flow through the NMOS devices to ground, causing nonadiabatic power dissipation. Although this loss is small in many technologies where V_{DD} is significantly higher than the threshold voltage, the process used in these experiments has a relatively large V_{th} to V_{DD} ratio.

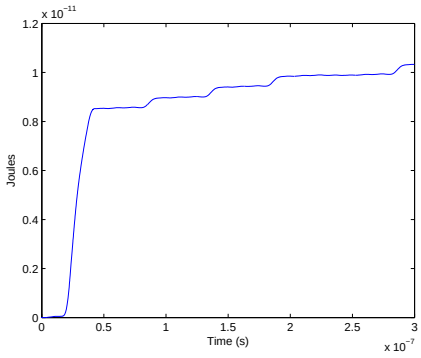

Figure 5: Power Consumption of ECRL Adder

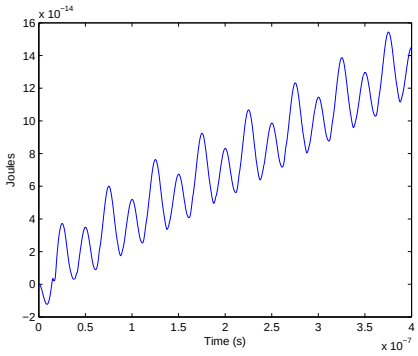

Figure 6: Power Consumption of PAL Adder

2.2.2 PAL

Pass transistor adiabatic logic (PAL), is another possible way to create adiabatic gates [3]. An example PAL gate is shown below in Figure (4). Like ECRL, PAL gates are also differential, but have the advantage of being able to be driven by just two sinusoidal power clocks, 180 degrees out of phase. As the power clock rises, the NMOS devices conduct and OUT begins to rise, and $\overline{OUT}$ remains near 0 V. Eventually the PMOS device will also conduct, charging the OUT to the peak of the power clock. As the power clock falls, the NMOS devices pull OUT back down to 0 V, recovering energy.

During simulation it was found that the value of $\overline{OUT}$ also rises and falls with the power clock, either due to leakage or capacitive feedthrough, but this did not adversely effect the operation of the adder. It is still possible to clearly distinguish when OUT is high and when $\overline{OUT}$ is high.

2.3 ECRL in sub-threshold

After analyzing the power consumption for both adiabatic and sub-threshold, we decided to run the adiabatic circuits sub-threshold to see if they would produce the correct output. This involved changing the four clocks to run below the threshold voltage. The value of V_{DD} was set to 240mV and 300mV on respective runs. Each ran for 1.5e-16 seconds. See figure (7.) As you can see there is a substantial difference between the power consumption for both 300mV and 240mV adiabatic simulations versus normal sub-threshold. One of the concerns noticed in the graph is that there is a

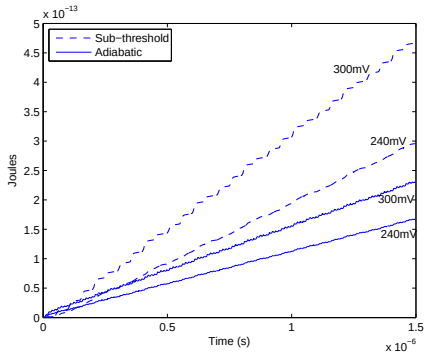

Figure 7: The graph shows the advantages of adiabatic sub-threshold over normally clocked sub-threshold

Table 1: Energy Consumption Per Addition

$V_{DD} = 1.0V$	296 fJ
$V_{DD} = 0.3V$	14 fJ
ECRL	425 fJ
PAL	16.3 fJ
ECRL, $V_{DD} = 0.3V$	9.6 fJ

ramp up power that occurs when the power turns on, even with this initialization there is a power save. Another aspect noticed when applying the sub-threshold application was that the solutions were one clock cycle off. The computations were correct but they came one cycle later. Given the dramatic power savings it seems worth it. The power savings for 300mV simulation was 50% more efficient than the sub-threshold counterpart. For 240mV there is a 40% power savings. This is assuming ideal clocks being generated.

3. CONCLUSION

Sub-threshold biasing proved to be a more effective technique for reducing power consumption than adiabatic charging. ECRL was particularly ineffective, giving worse performance than a standard adder biased at the default voltage. This is due to the increased ratio of V_{th} to V_{DD}, which causes non-adiabatic losses in the ECRL gates. The PAL gates do not have this limitation and compare favorably to the sub-threshold case in energy usage per addition. Sub-theshold, however, gives the best performance and is less complex than the adiabatic cases. Additionaly, our results show that adiabatic principles still apply even in the sub-threshold region, and the two techniques are not mutually exclusive.

Further research can be done to study effective adiabatic clock generation, as well as evaluating the effectiveness of the various adiabatic implimentations in the sub-threshold region.

4. REFERENCES

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